## REMARKS

The drawings were objected to. Please find attached drawings with the proposed changes indicated in red to Figures 3 and 7. These changes add no new matter as the reference to the substrate (195 in Figure 3) and the gate floating body connection (310 in Figure 7) is described in the specification as filed. The specification was amended to refer to the amended drawings.

Claims 1-3, 5-7, 9-11, and 13-15 were rejected under 35 U.S.C. 102(e) as being anticipated by Hagihara; Claims 1-3, 5-7, 9-11, and 13-15 were rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hagihara; and Claims 4, 8, 12, and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hagihara.

Hagihara discloses a block diagram in Figure 1 which is labeled a pull down network. Hagihara does not disclose a plurality of series connected MOS transistors wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series connected MOS transistors is a PMOS transistor as claimed in claim 1. The examiner states that "it is inherent that the transistors are connected in parallel or in series depending on whether the logic circuit is either MOR or NAND gate." There is no statement in the Hagihara patent describing or claiming a particular configuration in the labeled logic network. The applicants are not sure what the examiner means by inherent. The applicants therefore request that the examiner explain with particularity what the so called inherent connection of MOS transistors is. The same is true for independent claims 5, 9, and 13.

For a 102 reference to be valid each and every limitation of the instant invention must be found in the reference. The limitations of independent claims 1, 5, 9, and 13 are not found in the Hagihara patent. The examiner is requested to particularly point out where the limitations of the independent claims 1, 5, 9, and 13 are to be found in the Hagihara patent. As such claims 1, 5, 9, and 13 are allowable over the Hagihara patent.

In addition all dependent claims that depend on claim 1, , 5, 9, and 13 contain the limitations of these claims and are therefore allowable over Hagihara patent.

The claims of the instant invention do not claim minimizing physical size, reducing power consumption, and increasing speed. The applicants therefore do not understand the examiners rejection of claims 1-3, 5-7, 9-11, and 13-15 under 103(a) since the above mentioned factors are not subjects of the claims. Applicants must therefore conclude that claims 1-3, 5-7, 9-11, and 13-15 are allowable over the Hagihara patent.

Applicants assert that claims 4, 8, 12, and 16 are allowable over any art cited by the examiner. In his rejection under 103(a) the examiner refers to the floating substrate body of Hagihara. Applicants have failed to find a floating substrate body anywhere in the Hagihara patent. If a floating substrate body does not exist in the Hagihara then it cannot be obvious to tie a gate of the pull-down network to a floating substrate body of Hagihara as stated by the examiner. Applicants therefore maintain that claims 4, 8, 12, and 16 are allowable over the Hagihara patent.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

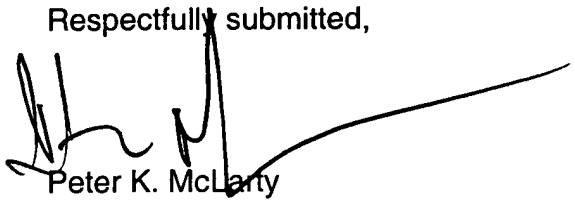
While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including

extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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## VERSION WITH MARKINGS TO SHOW CHANGES

### In the specification

As stated above, circuit performance of the dynamic SOI logic circuits of the instant invention can be improved using low threshold voltage techniques such as electrically connecting the transistor gate to the floating body of the SOI transistor. The gate-to-body connection can be applied to the PMOS transistors and NMOS transistors in a PDN. A gate to floating body connection 310 is shown in Figure 7 for a PMOS transistor in the PDN 267. The gate-to-body connection utilizes the body effect of the MOSFET transistor to lower the threshold voltage thus improving the transistor performance. The SOI dynamic logic circuits described in the instant invention can also be applied to bulk CMOS circuits. Thus the embodiments of the invention illustrated in Figures 4 – 7 can be applied to bulk substrates that do not have a buried dielectric layer. In the bulk CMOS embodiment of the instant invention, the source/drain diffusions of the PMOS transistor will not abut the source/drain diffusions of the NMOS transistor under current bulk CMOS transistor isolation schemes. The advantages gain by using the disclosed static logic design over existing bulk CMOS static logic designs will be in the speed and performance of the logic circuits.